

CLAIMS

- 1 1. A method for forming a transistor, the method comprising the steps of:
- 2 a) providing a semiconductor substrate;
- 3 b) patterning the semiconductor substrate to provide a first body edge;
- 4 c) providing a first gate structure of a first fermi level adjacent said first body
- 5 edge;
- 6 d) patterning the semiconductor substrate to provide a second body edge, the
- 7 first and second body edges of the semiconductor substrate defining a
- 8 transistor body; and
- 9 e) providing a second gate structure of a second fermi level adjacent said
- 10 second body edge.
- 1 2. The method of claim 1 wherein the first gate structure of a first fermi level
- 2 comprises p-type material and wherein the second gate structure of a second
- 3 fermi level comprises n-type material.
- 1 3. The method of claim 1 wherein the first gate structure of a first fermi level
- 2 comprises n-type material and wherein the second gate structure of a second
- 3 fermi level comprises p-type material.

1 4. The method of claim 1 wherein the semiconductor substrate comprises a
2 silicon-on-insulator layer, and wherein the step of patterning the
3 semiconductor substrate to provide a first body edge comprises patterning the
4 silicon-on-insulator layer and wherein the step of patterning the semiconductor
5 substrate to provide a second body edge comprises patterning the silicon-on-
6 insulator layer.

1 5. The method of claim 1 further comprising the steps of forming a first gate
2 dielectric layer on the first body edge and forming a second gate dielectric
3 layer on the second body edge.

1 6. The method of claim 1 wherein the step of patterning the semiconductor
2 substrate to provide a first body edge comprises forming a mandrel layer on
3 the semiconductor substrate; patterning the mandrel layer to form an exposed
4 side, and forming a sidewall spacer adjacent to the exposed side, and wherein
5 a first edge of the sidewall spacer defines the first body edge.

1 7. The method of claim 6 wherein the step of patterning the semiconductor
2 substrate to provide a second body edge comprises using a second edge of the
3 sidewall spacer to define the second body edge.

1 8. The method of claim 1 further comprising the step of forming a source/drain
2 implant into the body of the transistor by performing an angled implant into
3 the transistor body.

1 9. The method of claim 1 further comprising the step of forming a substantially
2 uniform dopant concentration density in the transistor body.

1 10. The method of claim 9 wherein the step of forming a substantially uniform
2 dopant concentration density in the transistor body comprises performing a
3 plurality of angled implants into the body.

1 11. The method of claim 1 wherein the of forming a substantially uniform dopant
2 concentration density in the transistor body comprising forming a dopant
3 concentration between $0.3 N_A$ and $3 N_A$, where N_A is defined as:

$$4 \quad N_A = \frac{2\varepsilon_{ox}Eg}{Toxs} \cdot \frac{(Toxs + \lambda)}{\left[(Toxs) + Toxw + Tsi \cdot \frac{\varepsilon_{ox}}{\varepsilon_{si}} \right]^2} \quad \text{Eq. 2}$$

- 1 12. The method of claim 9 wherein the step of forming a substantially uniform
2 dopant concentration density in the transistor body comprises performing a
3 first angled implant when the first body edge is exposed and performing a
4 second angled implant when the second body edge is exposed.

- 1 13. The method of claim 11 wherein the first angled implant comprises an implant
2 at approximately 45° with respect to the semiconductor substrate and wherein
3 the second angled implant comprises an implant at approximately 45° with
4 respect to the semiconductor substrate.

- 1 14. The method of claim 1 wherein the step of patterning the semiconductor
2 substrate to provide a first body edge comprises forming a mandrel layer on
3 the semiconductor substrate; patterning the mandrel layer, and using the
4 patterned mandrel layer to define the first body edge.

- 1 15. The method of claim 14 wherein the step of patterning the semiconductor
2 substrate to provide a second body edge comprises forming a sidewall spacer
3 adjacent to a gate material layer and using the sidewall spacer to define the
4 second body edge.

1 18. The method of claim 16 wherein the first gate structure of a first fermi level
2 comprises n-type polysilicon material and wherein the second gate structure of
3 a second fermi level comprises p-type polysilicon material.

1 19. The method of claim 16 further comprising the step of forming a source/drain
2 implant into the body of the transistor by performing an angled implant into
3 the transistor body.

1 20. The method of claim 16 wherein the step of depositing sidewall spacer
2 material in sidewall spacer trough comprises forming a sidewall oxide layer in
3 said trough, forming a nitride layer over said sidewall oxide layer, and filling
4 said sidewall spacer trough with a deposition of oxide.

1 21. The method of claim 16 further comprising the step of forming a substantially
2 uniform dopant concentration density in the transistor body.

- 1 25. A transistor comprising:
- 2 a) a transistor body formed on a substrate, the transistor body having a first
- 3 vertical edge and a second vertical edge;
- 4 b) a first gate structure adjacent the transistor body first vertical edge, the first
- 5 gate structure having a first fermi level; and
- 6 c) a second gate structure adjacent the transistor body second vertical edge, the
- 7 second gate structure having a second fermi level.
- 1 26. The transistor of claim 25 wherein the first gate structure comprises p-type
- 2 material and wherein the second gate structure comprises n-type material.
- 1 27. The transistor of claim 25 wherein the first gate structure comprises n-type
- 2 material and wherein the second gate structure comprises p-type material.
- 1 28. The transistor of claim 25 wherein the transistor body comprises a portion of
- 2 a silicon-on-insulator layer.
- 1 29. The transistor of claim 25 wherein the first and second gate structures
- 2 comprise polysilicon.

1 30. The transistor of claim 25 further comprising a first gate dielectric between the
2 transistor body first edge and the first gate structure and a second gate
3 dielectric between the transistor body second edge and the second gate
4 structure.

1 31. The transistor of claim 25 wherein the transistor body comprises a
2 source/drain implant into the transistor body.

1 32. The transistor of claim 25 wherein the transistor body has a substantially
2 uniform dopant concentration density.

1 33. The transistor of claim 32 wherein the substantially uniform dopant
2 concentration density is comprises a plurality of angled implants into the
3 transistor selected to result in a substantially uniform dopant concentration
4 density.

- 1 34. The transistor of claim 32 wherein the substantially uniform dopant
 2 concentration comprises a dopant concentration between $0.3 N_A$ and $3 N_A$,
 3 where N_A is defined as:

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$$N_A = \frac{2\epsilon_{ox}Eg}{Toxs} \cdot \frac{(Toxs + \lambda)}{\left[(Toxs) + Toxw + Tsi \cdot \frac{\epsilon_{ox}}{\epsilon_{si}} \right]^2} \quad \text{Eq. 2}$$

- 1 35. The transistor of claim 25 wherein the transistor body first edge is opposite the
 2 transistor body second edge and wherein the transistor body first edge and
 3 transistor body second edge are substantially perpendicular to a top surface of
 4 the substrate.

- 1 36. A double gated field effect transistor comprising:
 - 2 a) a transistor body, the transistor body formed from a silicon layer formed
 - 3 above an insulator layer , the transistor body having a first vertical edge and a
 - 4 vertical second edge, wherein the transistor body first edge and the transistor
 - 5 body second edge are opposite each other and substantially perpendicular to
 - 6 the insulator layer;
 - 7 b) a first gate dielectric layer formed on the transistor body first edge;
 - 8 c) a second gate dielectric layer formed on the transistor body second edge;
 - 9 d) a first gate structure formed on the first gate dielectric layer adjacent to the
 - 10 transistor body first edge, the first gate structure comprising p-type
 - 11 polysilicon; and
 - 12 e) a second gate structure formed on the second gate dielectric layer adjacent
 - 13 to the transistor body second edge, the second gate structure comprising n-type
 - 14 polysilicon.

- 1 37. The double gated field effect transistor of claim 36 further comprising a
- 2 source/drain implant in the transistor body formed by performing an angled
- 3 implant into the transistor body.

- 1 38. The double gated field effect transistor of claim 36 wherein the body
- 2 comprises a substantially uniform dopant concentration density.

- 1 39. The double gated field effect transistor of claim 38 wherein the substantially
2 uniform dopant concentration density is formed by performing a plurality of
3 angled implants into the transistor body.
- 1 40. The double gated field effect transistor of claim 36 further comprising a
2 polysilicon plug to electrically couple the first gate structure to the second gate
3 structure.
- 1 41. A method for forming a semiconductor device, the method comprising the
2 steps of:
3 a) forming a single crystal semiconductor fin having a first side and a second
4 side;
5 b) tilt implanting said first side of the single crystal semiconductor fin and tilt
6 implanting said second side of the single crystal semiconductor fin.
- 1 42. The method of claim 41 wherein the step of forming a single crystal
2 semiconductor fin comprises patterning a silicon on insulator layer to define a
3 transistor body.

1 43. The method of claim 41 further comprising the step of providing a first gate
2 structure of a first fermi level adjacent said first said and providing a
3 providing a second gate structure of a fermi level function adjacent said
4 second side.

1 44. The method of claim 43 wherein the first gate structure of a first fermi level
2 comprises p-type material and wherein the second gate structure of a second
3 fermi level comprises n-type material.

1 45. The method of claim 43 further comprising the steps of forming a first gate
2 dielectric layer on the first side and forming a second gate dielectric layer on
3 the second side.

1 46. The method of claim 41 wherein the step of forming the single crystal
2 semiconductor fin comprises forming a mandrel layer on a semiconductor
3 layer; patterning the mandrel layer to form an exposed side, wherein the
4 exposed side of the mandrel layer defines the first side of the single crystal
5 semiconductor fin.

